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10/584,620	06/26/2006	Eiichi Sadayuki	28951.1179	8160

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EXAMINER	
WILLIAMS, ARUN C	

ART UNIT	PAPER NUMBER
2838	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/584,620	SADAYUKI ET AL.	
	Examiner	Art Unit	
	ARUN WILLIAMS	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6/26/2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *6/26/2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/26/2006,7/1/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

2. Applicant is reminded of the proper content of an abstract of the disclosure.

A patent abstract is a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains. If the patent is of a basic nature, the entire technical disclosure may be new in the art, and the abstract should be directed to the entire disclosure. If the patent is in the nature of an improvement in an old apparatus, process, product, or composition, the abstract should include the technical disclosure of the improvement. In certain patents, particularly those for compounds and compositions, wherein the process for making and/or the use thereof are not obvious, the abstract should set forth a process for making and/or use thereof. If the new technical disclosure involves modifications or alternatives, the abstract should mention by way of example the preferred modification or alternative.

The abstract should not refer to purported merits or speculative applications of the invention and should not compare the invention with the prior art.

Where applicable, the abstract should include the following:
(1) if a machine or apparatus, its organization and operation;
(2) if an article, its method of making;
(3) if a chemical compound, its identity and use;
(4) if a mixture, its ingredients;
(5) if a process, the steps.

Extensive mechanical and design details of apparatus should not be given.

Drawings

3. Figures 11 and 12 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct

any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the third comparator must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

5.

Claim Objections

6. Claim 4 is objected to because of the following informalities: Claim 4 recites, "first comparator r the" is unclear. Appropriate correction is required.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1 and 3 are rejected under 35 U.S.C. 102(b) as being anticipated by Murayama et al, (Murayama), USPAT6,118,295 .

As for claim 1, Murayama discloses and shows in Fig. 1 a semiconductor device comprising: a capacitance (c1) element one end of which is connected to a power supply (Vdd); a first comparator(11) which has two input nodes having opposite polarity to each other and receives a reference voltage (VA) and an output of the other end of the capacitance element at their inputs to compare the respective voltage values to output a signal indicating a comparison result; a first resister (R1) element which connects the one side input node and the other side input node of the first comparator; and wherein the first comparator activates the output signal indicating the comparison result when the voltage difference between the inputted reference voltage and the inputted output of the other end of the capacitance element occurs power supply voltage varies. (col.2-3, lines 66-16)

As for claim 3, Murayama a second (R2) and third resister (R3) elements connected in series between the power supply voltage and the ground terminal to divide the power supply voltage; a second comparator (12) having two input nodes and receives the voltage divided by the second and the third resister elements and the reference voltage at its inputs to compare those; and a logic OR circuit (13) which takes a logic OR operation of the output signal of the first comparator and the output signal of the second comparator.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

11. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein

were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

12. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murayama in view of Dancy et al,(Dancy), USPAT6,577,109.

As for claim 2, Murayama differs from the claimed invention because he does not explicitly disclose a hysteresis comparator which activates the output signal indicating the comparison result when the voltage difference between the inputted reference voltage and the inputted output of the other end of the capacitance element becomes larger than a predetermined hysteresis width.

Dancy discloses and shows in Fig. 9 a hysteresis comparator (901)which activates the output signal indicating the comparison result when the voltage difference between the inputted reference voltage and the inputted output of the other end of the capacitance element becomes larger than a predetermined hysteresis width (col.10, lines 12-23)

Dancy is evidence that ordinary skill in the art would find a reason, suggestion or motivation to use a hysteresis comparator which activates the output signal indicating the comparison result when the voltage difference between the inputted reference voltage and the inputted output of the other end of the capacitance element becomes larger than a predetermined hysteresis width

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify Murayama by a hysteresis comparator which activates the output signal indicating the comparison result when the voltage difference between the inputted reference voltage and the inputted output of the other end of the capacitance element becomes larger than a predetermined hysteresis widthfor advantages such as providing the ability of an adjustable comparator(col.10, lines 12-23), as taught by Dancy.

13. Claims 4,5, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murayama in view of Massie et al, (Massie), USPAT 6,271,650

As for claims 4,5, and 6, Murayama differs from the claimed invention because he does not explicitly disclose a reset portion.

Massie discloses and shows in Fig. 9 a reset portion (119) which received the output signals of the first comparator, and stops the operation of the system including the semiconductor device when the output signal of the first comparator r the output signal of the second comparator is activated (col.5, lines 10-29). Furthermore, Massie discloses and shows in Fig. 3 a switching part (307) and a control section (305)

Massie is evidence that ordinary skill in the art would find a reason, suggestion or motivation to use a reset portion which received the output signals of the first comparator, and stops the operation of the system including the semiconductor device when the output signal of the first comparator r the output signal of the second comparator is activated

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify Murayama by using a reset portion which received the output signals of the first comparator, and stops the operation of the system including the semiconductor device when the output signal of the first comparator r the output signal of the second comparator is activated for advantages such as providing the ability of an adjustable comparator(col.5, lines 10-29), as taught by Massie.

14. Claims 7-9,11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murayama in view of Venema, USPAT4,633,168

As for claim 7, Murayama differs from the claimed invention because he does not explicitly disclose a first and second capacitance elements one end of each of which is connected to a power supply.

Venema discloses and shows in Fig. 1 a first (C1) and second (C2) capacitance elements one end of each of which is connected to a power supply.

Venema is evidence that ordinary skill in the art would find a reason, suggestion or motivation to use a first and second capacitance elements one end of each of which is connected to a power supply.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify Murayama by using a first and second capacitance elements one end of each of which is connected to a power supply for advantages such as providing the ability to determine capacitance (col.1, lines 28-30) , as taught by Venema.

As for claim 8, see rejection for claim 2.

As for claim 9, Murayama discloses and shows in Fig. 1 a third (R3) and fourth (R4) resister elements connected in series between the power supply and the ground terminal to divide the power supply voltage; and a third comparator which has two input nodes and compares the voltage which is divided by a-third and a-fourth resister elements and the reference voltage to output a signal indicating the comparison result to the logic OR circuit (13).

As for claims 11 and 12, see rejections for claim 5 and 6 respectively.

15. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murayama in view of Park, USPAT6,229,775

As for claim 10, Murayama differs from the claimed invention because he does not explicitly disclose a reset part which receives the output signal of the logic OR circuit at its input and stops the operation of a system including the semiconductor device when the output signal of the first comparator, the second comparator, or the third comparator is activated.

Park discloses and shows in Fig. 6 a reset part (604) which receives the output signal of the logic OR circuit (603) its input and stops the operation of a system including the semiconductor device when the output signal of the first comparator, the second comparator, or the third comparator is activated.

Park is evidence that ordinary skill in the art would find a reason, suggestion or motivation to use a reset part which receives the output signal of the logic OR circuit at its input and stops the operation of a system including the semiconductor device when

the output signal of the first comparator, the second comparator, or the third comparator is activated.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify Murayama by using a reset part which receives the output signal of the logic OR circuit at its input and stops the operation of a system including the semiconductor device when the output signal of the first comparator, the second comparator, or the third comparator is activated for advantages such as providing the ability to discriminate signals (col.2, lines 53-55) , as taught by Park.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arun Williams whose telephone number is 571-272-9765. The examiner can normally be reached on Mon - Thrus,6:30am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Akm Ullah can be reached on 571-272-2361. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Akm Enayet Ullah/
Supervisory Patent Examiner, Art Unit 2838

Arun Williams
Examiner
Art Unit 2838

/A. W./
Examiner, Art Unit 2838

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IN THE CLAIMS:

1.

(Currently Amended) A semiconductor device comprising:

a capacitance element one end of which is connected to a power supply; a first comparator which has two input nodes having opposite polarity to each other and receives a reference voltage and ~~a power supply voltage~~ an output of the other end of the capacitance element at their inputs to compare the respective voltage values to output a signal indicating a comparison result;

a first resister element which connects the one side input node and the other side input node of the first comparator; and

~~a capacitance element one end of which is connected to a power supply terminal which applies said power supply voltage and the other end of which ig connected to the one side input node of the comparator~~

wherein the first comparator activates the output signal indicating the comparison result when the voltage difference between the inputted reference voltage and the inputted output of the other end of the capacitance element occurs power supply voltage varies.

2.

(Currently Amended) A semiconductor device as defined in claim 1,

wherein:

the first comparator is a hysteresis comparator which activates the output signal indicating the comparison result when the voltage difference between the inputted reference voltage and the ~~power supply voltage~~ inputted output of the other end of the capacitance element becomes larger than a predetermined hysteresis width.

3.

(Currently Amended) A semiconductor device as defined in claim 1, wherein further comprising:

a second and third resister elements connected in series between the power supply ~~terminal~~ voltag_e and the ground terminal to divide the power supply voltage;

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a second comparator having two input nodes and receives the ~~power supply voltage~~ voltage divided by the second and the third resister elements and the reference voltage at its inputs to compare those; and

a logic OR circuit which takes a logic OR operation of the output signal of the first comparator and the output signal of the second comparator.

4.

(Currently Amended) A semiconductor device as defined in claim 3 any of the ~~claimg 1-3,~~ wherein further comprising:

a reset portion which received the output signals of the first comparator or the logic OR

circuit at their inputs, and stops the operation of the system including the semiconductor device when the output signal of the first comparator r the output signal of the second comparator is activated.

5.

(Currently Amended) A semiconductor device as defined in claim 3 ~~any of the claimg 1-3,~~ wherein further comprising:

a switching part which switches the value of the ~~power gupply voltage~~ output of the other end of the capacitance element which is inputted to either of the input nodes of the first comparator to an arbitrary value.

6.

(Original)

Semiconductor device as defined in claim 5, wherein further comprising:

a control section which operates the switching part at turning on the power of the semiconductor device.

7.

(Currently Amended) A semiconductor device comprising:

first and second capacitance elements one end of each of which is connected to a power

su_p_p_ l;

a first ~~and a second comparatorg each~~ of comparator which has two input nodes having

opposite polarity to each other and ~~receives a~~ receiving reference voltage and ~~a~~ ~~powersupply~~

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~~voltage~~ an output of the other end of the first capacitance element at their inputs to compare the respective voltage values to output a signal indicating a comparison result;

a second comparator which has two input nodes having opposite polarity to each other and receiving a reference voltage and an output of the other end of the second capacitance element at their inputs to compare the respective voltage values to output a signal indicating a comparison result;

a first and a second resister elements each of which connects the one side input node and the other side input node of the first and the second comparators, respectively~

~~a first and a second capacitance elements, one end of which is both connected to a power supply terminal which applies said power supply voltage, and the other end of which is connected to the one side input node of the first and the second comparator, respectively;~~

alogic OR circuit which takes a logic OR operation of the output signal of the first comparator and the output signal of the second comparator; and

wherein the first and the second comparators respectively activate the output signal indicating the comparison results when the voltage difference between the inputted reference

• voltage and the power ~~supply voltage varies~~ inputted output of the other end of the capacitance element occurs, and the polarity of the input node which receives the ~~power supply voltage~~ output of the other end of the first capacitance element in the first comparator and the polarity of the input node which receives ~~the power supply voltage~~ an output of the other end of the second capacitance element in the second comparator are opposite to each other.

8.

(Currently Amended) A semiconductor device as defined as defined in claim 7 wherein:

the first comparator and the second comparator respectively are hysteresis comparators which ~~activates~~ activate the output signal indicating the comparison result when the voltage difference between the inputted reference voltage and the ~~power supply voltage~~ inputted output of the other end of the first capacitance element is larger than a predetermined hysteresis width.

9.

(Currently Amended) A semiconductor device as defined in claim 7, wherein further comprising:

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a third and fourth resister elements connected in series between the power supply ~~tern-final~~ and the ground terminal to divide the power supply voltage; and

a third comparator which has two input nodes and compares the ~~power supply~~ voltage which is divided by a-third and a-fourth resister elements and the reference voltage to output a signal indicating the comparison result to the logic OR circuit.

10. (Currentiy Amended) A semiconductor device as defined in ~~any of claims 7 to 9~~ claim 9, wherein:

there is further provided a reset part which receives the output signal of the logic OR circuit at its input and stops the operation of a system including the semiconductor device when the output signal of the first comparator, the second comparator, or the third comparator is activated.

11. (Currently Amended) A semiconductor device as defined in ~~any of claims 7 to 9~~ claim 9, ~~wherein~~ further comprising:

a switching part which switches the value of the ~~power supply voltage~~ output of the

other end of the first capacitance element which is inputted to either of the input nodes of the first ~~and the second comparators~~ comparator and the value of the output of the other end of the second capacitance element which is inputted to either of the input nodes of the second comparator to an arbitrary value.

12. (Currently Amended) semiconductor device as defined in claim 11 ~~wherein~~ further comprising:

a control section which operates the switching part at turning on the power of the semiconductor device.